

AMENDMENTS TO THE CLAIMS

Claims 1-35. (Canceled)

36. (Currently amended) A memory cell comprising:

a transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate;

an insulating layer provided over said substrate; and

a container capacitor including a first metal barrier layer, a lower electrode over said first metal barrier layer, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer, said upper electrode comprising doped polysilicon, and said lower electrode having a surface aligned over said source/drain region,

wherein said lower electrode comprises an electropolished patterned metal layer which is situated fully within said insulating layer,

wherein said first metal barrier layer is fully within said insulating layer,

wherein said electropolished patterned metal layer has a thickness of about 50 to about 300 Angstroms,

and wherein said dielectric layer is in contact with said insulating layer.

37. (Original) The memory cell of claim 36, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

38. (Original) The memory cell of claim 37, wherein said electropolished patterned metal layer contains a noble metal.

39. (Original) The memory cell of claim 38, wherein said electropolished patterned metal layer is a platinum layer.

Claim 40. (Canceled)

41. (Previously presented) The memory cell of claim 36, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

Claim 42-43. (Canceled)

44. (Currently amended) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and said processor comprising a container capacitor provided within an insulating layer, said container capacitor including a first metal barrier layer, a lower electrode and an upper electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms, wherein a top surface of said electropolished patterned metal layer and said first metal barrier layer are [[is]] at the same level with a top surface of said insulating layer such that said lower electrode and said first metal barrier layer do[[es]] not extend above the top surface of said insulating layer, and said upper electrode comprising doped polysilicon.

45. (Original) The processor-based system of claim 44, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

46. (Original) The processor-based system of claim 45, wherein said electropolished patterned metal layer contains a noble metal.

47. (Original) The processor-based system of claim 46, wherein said electropolished patterned metal layer is a platinum layer.

Claim 48. (Canceled)

49. (Original) The processor-based system of claim 44, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

Claim 50. (Canceled)

51. (Original) The processor-based system of claim 44, wherein said integrated circuit is a memory module.

52. (Original) The processor-based system of claim 51, wherein said memory module is a DRAM memory.

53. (Original) The processor-based system of claim 51, wherein said memory module is a SRAM memory.

54. (Original) The processor-based system of claim 51, wherein said memory module is a MCM memory.

55. (Currently amended) A container capacitor comprising:

a first metal barrier layer provided fully within a first insulating layer, said barrier layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom;

a lower electrode provided fully within [[a]] said first insulating layer and over said first metal barrier layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom;

a second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer; and

an upper electrode provided over said second insulating layer.

56. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

57. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer has a thickness of approximately 50 to 300 Angstroms.

58. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

59. (Previously presented) A container capacitor comprising:

an insulating layer provided over a substrate, said insulating layer containing an opening;
a tantalum nitride barrier conductive layer provided at a bottom of said opening;

a lower electrode provided over said tantalum nitride barrier conductive layer, said lower electrode comprising an electropolished patterned metal layer having a bottom and vertical sidewalls extending upwardly from said bottom such that said lower electrode is situated fully within said insulating layer, said lower electrode having a thickness of approximately 100 Angstroms;

a dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer; and

an upper electrode comprising doped polysilicon provided over said dielectric material and wherein said lower electrode, said dielectric material and said upper electrode form said container capacitor.

Claims 60-64. (Canceled)

65. (Previously presented) A capacitor structure comprising:

an insulating layer provided over a substrate, the insulating layer including a contact opening, the contact opening having a first height;

a barrier conductive layer provided within the contact opening, the barrier conductive layer being disposed along a bottom and sidewalls of the contact opening, wherein the barrier conductive layer has a first thickness and wherein a length of upwardly extending portions of the

barrier conductive layer that are disposed along the sidewalls of the contact opening is equal to the first height;

a lower platinum electrode provided over the barrier conductive layer, the lower platinum electrode being disposed along a bottom portion and sidewall portions of the barrier conductive layer, wherein a length of upwardly extending portions of the lower platinum electrode that are disposed along the sidewall portions of the barrier conductive layer is equal to the first height minus the first thickness;

a dielectric layer provided over the lower platinum electrode, the dielectric layer being disposed along a bottom portion and sidewall portions of the lower platinum electrode and on an upper surface of the barrier conductive layer and an upper surface of the substrate; and

a second platinum electrode provided over the dielectric layer, the second platinum electrode being disposed along a bottom portion, sidewall portions and an upper surface of the dielectric layer.

66. (New) The memory cell of claim 36, further comprising a second metal barrier layer below and in contact with the first metal barrier layer.

67. (New) The processor-based system of claim 44, wherein the integrated circuit further comprises a second metal barrier layer below and in contact with the first metal barrier layer.

68. (New) The container capacitor of claim 55, further comprising a second metal barrier layer below and in contact with the first metal barrier layer.

69. (New) The capacitor structure of claim 65, further comprising a metal barrier layer below and in contact with the barrier conductive layer.

70. (New) The container capacitor of claim 59, further comprising a metal barrier layer below and in contact with the tantalum nitride barrier conductive layer.

71. (New) The container capacitor of claim 59, wherein said electropolished patterned lower electrode contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

72. (New) The container capacitor of claim 59, wherein said electropolished patterned lower electrode contains a noble metal.

73. (New) The container capacitor of claim 59, wherein said electropolished patterned lower electrode is a platinum layer.